METHODS OF FABRICATING GALLIUM NITRIDE MICROELECTRONIC LAYERS ON SILICON LAYERS AND GALLIUM NITRIDE MICROELECTRONIC STRUCTURES FORMED THEREBY

Cross-Reference to Provisional Applications

This application claims the benefit of Provisional Application Serial No. 60/109,674, filed November 24, 1998 entitled *Methods for Growing Low Defect*

5   *Gallium Nitride Semiconductor Layers on Silicon or Silicon Containing Wafers Using a Conversion and Lateral Epitaxial Overgrowth Transition Structure and Gallium Nitride Semiconductor Structures Fabricated Thereby* and Provisional Application Serial No. 60/109,860 filed November 24, 1998 entitled *Pendeo-Epitaxial Methods of Fabricating Gallium Nitride Semiconductor Layers on Silicon Wafers or Wafers*

10   *Containing Silicon, and Gallium Nitride Semiconductor Structures Fabricated Thereby.*

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Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and

20   more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices

25   including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium

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nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It also is known to produce low defect density gallium nitride layers by forming a mask on a layer of gallium nitride, the mask including at least one opening that exposes the underlying layer of gallium nitride, and laterally growing the underlying layer of gallium nitride through the at least one opening and onto the mask. This technique often is referred to as "Epitaxial Lateral Overgrowth" (ELO). The layer of gallium nitride may be laterally grown until the gallium nitride coalesces on the mask to form a single layer on the mask. In order to form a continuous layer of gallium nitride with relatively low defect density, a second mask may be formed on the laterally overgrown gallium nitride layer, that includes at least one opening that is offset from the underlying mask. ELO then again is performed through the openings in the second mask to thereby overgrow a second low defect density continuous gallium nitride layer. Microelectronic devices then may be formed in this second overgrown layer. ELO of gallium nitride is described, for example, in the publications entitled *Lateral Epitaxy of Low Defect Density GaN Layers Via Organometallic Vapor Phase Epitaxy* to Nam et al., Appl. Phys. Lett. Vol. 71, No. 18, November 3, 1997, pp. 2638-2640; and *Dislocation Density Reduction Via Lateral Epitaxy in Selectively Grown GaN Structures* to Zheleva et al, Appl. Phys. Lett., Vol. 71, No. 17, October 27, 1997, pp. 2472-2474, the disclosures of which are hereby incorporated herein by reference.

It also is known to produce a layer of gallium nitride with low defect density by forming at least one trench or post in an underlying layer of gallium nitride to define at least one sidewall therein. A layer of gallium nitride is then laterally grown from the at least one sidewall. Lateral growth preferably takes place until the laterally grown layers coalesce within the trenches. Lateral growth also preferably

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continues until the gallium nitride layer that is grown from the sidewalls laterally overgrows onto the tops of the posts. In order to facilitate lateral growth and produce nucleation of gallium nitride and growth in the vertical direction, the top of the posts and/or the trench floors may be masked. Lateral growth from the sidewalls of

5   trenches and/or posts also is referred to as "pendeoepitaxy" and is described, for example, in publications entitled *Pendeo-Epitaxy: A New Approach for Lateral Growth of Gallium Nitride Films* by Zheleva et al., Journal of Electronic Materials, Vol. 28, No. 4, February 1999, pp. L5-L8; and *Pendeoepitaxy of Gallium Nitride Thin Films* by Linthicum et al., Applied Physics Letters, Vol. 75, No. 2, July 1999, pp.

10   196-198, the disclosures of which are hereby incorporated herein by reference.

ELO and pendeoepitaxy can provide relatively large, low defect gallium nitride layers for microelectronic applications. However, a major concern that may limit the mass production of gallium nitride devices is the growth of the gallium nitride layers on a silicon carbide substrate. Notwithstanding silicon carbide's

15   increasing commercial importance, silicon carbide substrates still may be relatively expensive compared to conventional silicon substrates. Moreover, silicon carbide substrates generally are smaller than silicon substrates, which can reduce the number of devices that can be formed on a wafer. Moreover, although large investments are being made in silicon carbide processing equipment, even larger investments already

20   have been made in conventional silicon substrate processing equipment. Accordingly, the use of an underlying silicon carbide substrate for fabricating gallium nitride microelectronic structures may adversely impact the cost and/or availability of gallium nitride devices.

Summary of the Invention

25   The present invention provides methods of fabricating a gallium nitride microelectronic layer by converting a surface of a (111) silicon layer to 3C-silicon carbide. A layer of 3C-silicon carbide is then epitaxially grown on the converted surface of the (111) silicon layer. A layer of 2H-gallium nitride then is grown on the epitaxially grown layer of 3C-silicon carbide. The layer of 2H-gallium nitride then is

30   laterally grown to produce the gallium nitride microelectronic layer.

In one embodiment, the silicon layer is a (111) silicon substrate, the surface of which is converted to 3C-silicon carbide. In another embodiment, the (111) silicon layer is part of a Separation by IMplanted OXygen (SIMOX) silicon substrate which includes a layer of implanted oxygen that defines the (111) layer on the (111) silicon

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substrate. In yet another embodiment, the (111) silicon layer is a portion of a Silicon-On-Insulator (SOI) substrate in which a (111) silicon layer is bonded to a substrate. Accordingly, the present invention can use conventional bulk silicon, SIMOX and SOI substrates as a base or platform for fabricating a gallium nitride microelectronic layer. By using conventional silicon technology, low cost and/or large area silicon substrates may be used and conventional silicon wafer processing systems also may be used. Accordingly, low cost and/or high volume production of gallium nitride microelectronic layers may be provided.

The surface of the (111) silicon layer preferably is converted to 3C-silicon carbide by chemically reacting the surface of the (111) silicon layer with a carbon containing precursor such as ethylene, to convert the surface of the (111) silicon layer to 3C-silicon carbide. The layer of 3C-silicon carbide then may be epitaxially grown on the converted surface using standard vapor phase epitaxial techniques for silicon carbide. Alternatively, the layer of 3C-silicon carbide may be grown directly on the (111) silicon layer, without the need for conversion. The epitaxially grown layer of 3C-silicon carbide may be thinned. Prior to growing the layer of gallium nitride, an aluminum nitride and/or gallium nitride buffer layer preferably is grown on the epitaxially grown layer of 3C-silicon carbide. The gallium nitride then is grown on the buffer layer, opposite the epitaxially grown layer of 3C-silicon carbide.

Lateral growth of the layer of 2H-gallium nitride may be performed by ELO wherein a mask is formed on the layer of 2H-gallium nitride, the mask including at least one opening that exposes the layer of 2H-gallium nitride. The layer of 2H-gallium nitride then is laterally grown through the at least one opening and onto the mask. A second, offset mask also may be formed on the laterally grown layer of 2H-gallium nitride and a second laterally grown layer of 2H-gallium nitride may be overgrown onto the offset mask. Lateral growth of the layer of 2H-gallium nitride also may be performed using pendeoepitaxial techniques wherein at least one trench and/or post is formed in a layer of 2H-gallium nitride to define at least one sidewall therein. The layer of 2H-gallium nitride then is laterally grown from the at least one sidewall. Pendeoepitaxial lateral growth preferably continues until the laterally grown sidewalls coalesce on the top of the posts or trenches. The top of the posts and/or the trench floors may be masked to promote lateral growth and reduce nucleation and vertical growth. The trenches preferably extend into the silicon carbide layer to also reduce nucleation and vertical growth.

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As described above, the present invention can use bulk silicon substrates, SIMOX substrates or SOI substrates as a platform for gallium nitride fabrication. Preferred methods using each of these substrates now will be described.

When using a (111) silicon substrate, the surface of the (111) silicon substrate preferably is converted to 3C-silicon carbide and a layer of 3C-silicon carbide then is epitaxially grown on the converted surface of the (111) silicon substrate. The epitaxially grown layer of 3C-silicon carbide may be thinned. An aluminum nitride and/or gallium nitride buffer layer is grown on the epitaxially grown layer of 3C-silicon carbide. A layer of 2H-gallium nitride is grown on the buffer layer. The layer of 2H-gallium nitride then is laterally grown to produce the gallium nitride microelectronic layer. The lateral growth may proceed using ELO, pendeoepitaxy and/or other techniques.

When using a SIMOX substrate, oxygen is implanted into a (111) silicon substrate to form a buried silicon dioxide layer that defines a (111) silicon surface layer on the (111) silicon substrate. At least a portion of the (111) silicon surface layer, and preferably all of the (111) silicon surface layer, is converted to 3C-silicon carbide. A layer of 3C-silicon carbide then is epitaxially grown on the converted (111) silicon surface layer. The epitaxially grown layer of 3C-silicon carbide then may be thinned and an aluminum nitride and/or gallium nitride buffer layer is grown on the epitaxially grown layer of 3C-silicon carbide. A layer of 2H-gallium nitride then is grown on the buffer layer. The layer of 2H-gallium nitride then is laterally grown, using ELO, pendeoepitaxy and/or other techniques to produce the gallium nitride microelectronic layer.

Finally, when using an SOI substrate, a (111) silicon substrate is bonded to another substrate, preferably a (100) silicon substrate. The (111) silicon substrate is thinned to define a (111) silicon layer on the (100) silicon substrate. At least a portion, and preferably all, of the (111) silicon layer is converted to 3C-silicon carbide. A layer of 3C-silicon carbide is epitaxially grown on the converted (111) silicon layer. The epitaxially grown layer of 3C-silicon carbide may be thinned and an aluminum nitride and/or gallium nitride buffer layer is grown on the epitaxially grown layer of 3C-silicon carbide. A layer of 2H-gallium nitride then is grown on the buffer layer and the layer of 2H-gallium nitride is laterally grown, using ELO, pendeoepitaxy and/or other techniques to produce the gallium nitride microelectronic layer. When using SOI substrates, microelectronic devices also may be formed in the

(100) silicon substrate, prior to or after forming the gallium nitride microelectronic layer. A portion of the (111) silicon layer, the 3C-silicon carbide layer, the gallium nitride layer and the gallium nitride microelectronic layer may be removed to expose the microelectronic devices in the (100) silicon substrate. Alternatively, an epitaxial

5   silicon layer may be grown from the exposed portion of the (100) silicon substrate, and microelectronic devices may be formed in the epitaxial silicon layer. The gallium nitride structures may be capped prior to forming the epitaxial silicon layer. Thus, for example, optoelectronic devices may be formed in the gallium nitride layer whereas conventional CMOS or other microelectronic devices may be formed in the (100)

10   silicon substrate. Integrated optoelectronic substrates thereby may be formed.

In general, gallium nitride microelectronic structures according to the present invention preferably comprise a (111) silicon layer, a 3C-silicon carbide layer on the (111) silicon layer, an underlying layer of 2H-gallium nitride on the 3C-silicon carbide layer and a lateral layer of 2H-gallium nitride on the underlying layer of 2H-

15   gallium nitride. The (111) silicon layer may comprise a surface of a (111) bulk silicon substrate, a surface of a (111) SIMOX substrate or a surface of a (111) SOI substrate. A buffer layer of aluminum nitride and/or gallium nitride may be provided between the 3C-silicon carbide layer and the underlying layer of 2H-gallium nitride. A mask may be provided on the underlying layer of 2H-gallium nitride, the mask

20   including at least one opening that exposes the underlying layer of 2H-gallium nitride, and the lateral layer of 2H-gallium nitride extending through the at least one opening and onto the mask. A second laterally offset mask and a second lateral layer of 2H-gallium nitride also may be provided. Alternatively or in addition, at least one trench and/or post may be provided in the underlying layer of 2H-gallium nitride that

25   defines at least one sidewall in the underlying layer of 2H-gallium nitride, and the lateral layer of 2H-gallium nitride may extend from the at least one sidewall. The lateral layer of 2H-gallium nitride may extend onto the post tops, which may be masked or unmasked. The trench bottoms also may be masked or the trench may extend through the aluminum nitride layer into the silicon carbide layer.

30   A preferred embodiment using a (111) bulk silicon substrate includes a 3C-silicon carbide layer on the (111) silicon substrate, a buffer layer of aluminum nitride and/or gallium nitride on the 3C-silicon carbide layer, an underlying layer of 2H-gallium nitride on the buffer layer and a lateral layer of 2H-gallium nitride on the underlying layer of 2H-gallium nitride. A preferred embodiment using a SIMOX

substrate includes a (111) silicon substrate, a silicon dioxide layer on the (111) silicon substrate, a 3C-silicon carbide layer on the silicon dioxide layer, a buffer layer of aluminum nitride and/or gallium nitride on the 3C-silicon carbide layer, an underlying layer of 2H-gallium nitride on the buffer layer and a lateral layer of 2H-gallium

5   nitride on the underlying layer of 2H-gallium nitride. Finally, a preferred embodiment using an SOI substrate includes a (100) silicon substrate, an insulating layer on the (100) silicon substrate, a 3C-silicon carbide layer on the insulating layer, a buffer layer of aluminum nitride and/or gallium nitride on the 3C-silicon carbide layer, an underlying layer of 2H-gallium nitride on the buffer layer and a lateral layer

10   of 2H-gallium nitride on the underlying layer of 2H-gallium nitride. A plurality of microelectronic devices preferably are formed in the (100) silicon substrate. The 3C-silicon carbide layer, the layer of aluminum nitride, the underlying layer of 2H-gallium nitride and the lateral layer of 2H-gallium nitride preferably define a pedestal that exposes the plurality of microelectronic devices in the (100) silicon substrate.

15   Alternatively, the pedestal may expose the (100) silicon substrate, substrate, a (100) silicon layer may be included on the exposed portion of the (100) silicon substrate, and the microelectronic devices may be formed in the (100) silicon layer. In all of the above embodiments, a layer of (111) silicon may be present between the insulating layer and the 3C-silicon carbide layer. Accordingly, gallium nitride microelectronic

20   structures may be formed on commonly used bulk silicon, SIMOX and SOI substrates. Low cost and/or high availability gallium nitride devices thereby may be provided. Integration with conventional CMOS or other silicon technologies also may be facilitated.

25   **Brief Description of the Drawings**

Figures 1-14 are cross-sectional views of first gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figures 16-26 are cross-sectional views of second gallium nitride microelectronic structures during intermediate fabrication steps, according to the

30   present invention.

Figures 27-41 are cross-sectional views of third gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

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Figures 42-43 are cross-sectional views of fourth gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figures 44-45 are cross-sectional views of fifth gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figure 46 is a cross-sectional view of sixth gallium nitride microelectronic structures according to the present invention.

Figures 47-49 are cross-sectional views of seventh gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or "onto" another element, it can be directly on the other element or intervening elements may also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figures 1-14, first embodiments of methods of fabricating gallium nitride microelectronic layers and microelectronic structures formed thereby are illustrated. Referring to Figure 1, a bulk silicon (111) substrate 102a is provided. The crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further. As shown in Figure 2, the surface of the (111) silicon substrate 102a preferably is converted to 3C-silicon carbide 102b. In particular, the surface of the silicon substrate 102a may be converted to 3C-silicon carbide by exposure to one or more carbon-containing sources. For example, a converted layer of 3C-SiC may be formed by heating the

bulk silicon substrate **102a** using ethylene at about 925°C for about fifteen minutes at a pressure of about 5E-5 Torr. More preferably, an ethylene flow rate of about 0.5sccm is used while heating the substrate from room temperature to about 925°C at a ramp up rate of about 30°C per minute and holding at about 925°C for about fifteen

5   minutes and at about 5E-5 Torr, resulting in a thin, 50 Ångstrom, 3C-silicon carbide layer **102b**.

Then, referring to Figure 3, a layer of 3C-silicon carbide **102c** may be formed on the converted 3C-silicon carbide layer **102b** using conventional vapor phase epitaxial techniques. For example, the silicon carbide layer may be grown using

10   propane (about 15% in hydrogen) and silane (about 5% in hydrogen) at about 1360°C and about 760 Torr. More preferably, propane (about 15% in hydrogen) at about 25 sccm, silane (about 5% in hydrogen) at about 100 sccm and hydrogen gas at about 2500 sccm at a temperature of about 1360°C and pressure of about 760 Torr may be used. It will be understood that the surface of the silicon substrate need not be

15   converted to 3C-silicon carbide prior to forming silicon carbide layer **102c**. Rather, layer **102c** may be formed directly on the silicon substrate **102a**.

Then, referring to Figure 4, the epitaxially grown layer of 3C-silicon carbide **102c** may be thinned, for example, to a thickness of about 0.5μm, to form a thin layer **102c'** of 3C-silicon carbide. Thinning may take place using chemical mechanical

20   polishing. The thinning may promote the formation of a smooth, defect free nucleation surface for 2H-aluminum nitride as will be described below. However, it will be understood that the 3C-silicon carbide layer **102c** need not be thinned.

Referring now to Figure 5, a buffer layer of 2H-aluminum nitride and/or gallium nitride **102d** then is grown on the epitaxially grown layer of 3C-silicon

25   carbide **102c** or **102c'**. The aluminum nitride layer **102d** may be about 0.01μm thick and may be formed using conventional techniques such as metalorganic vapor phase epitaxy. It also will be understood that the buffer layer of aluminum nitride and/or gallium nitride **102d** need not be included, and gallium nitride may be formed directly on the epitaxially grown layer **102c/102c'** of 3C-silicon carbide. The combination of

30   the (111) silicon substrate **102a**, the silicon carbide layers **102b** and **102c'** and the buffer layer **102d** forms a platform **102** upon which a gallium nitride microelectronic layer may be fabricated. Thus, as shown in Figure 6, an underlying 2H-gallium nitride layer **104** is grown on the 2H-aluminum nitride layer **102d**. The gallium nitride layer **104** may be between about 0.5 and about 2.0μm thick and may be grown

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at about 1000°C in a cold wall vertical and inductively heated metal organic vapor phase epitaxy system using triethyl gallium at about 26 mμmol/min, ammonia at about 1500 sccm and about 3000 sccm hydrogen diluent. Additional details of the growth technique for the aluminum nitride layer **102d** and the gallium nitride layer

5   **104** may be found in a publication by T. W. Weeks et al. entitled *"GaN Thin Films Deposited Via Organometallic Vapor Phase Epitaxy on α(6H)-SiC(0001) Using High-Temperature Monocrystalline AlN Buffer Layers"*, Applied Physics Letters, Vol. 67, No. 3, July 17, 1995, pp. 401-403.

Referring now to Figures 7-14, gallium nitride microelectronic layers may be

10   fabricated on the underlying gallium nitride layer **104** using ELO. It also will be understood, however, that gallium nitride microelectronic layers may be fabricated using pendeoepitaxy as will be described in connection with other embodiments of the invention and/or using other techniques for fabricating gallium nitride microelectronic layers.

15   Referring to Figure 7, the underlying gallium nitride layer **104** is masked with a first mask **106** that includes a first array of openings **107** therein. The first mask may comprise silicon dioxide at a thickness of 1000Å and may be deposited using Low Pressure Chemical Vapor Deposition (LPCVD) at 410°C. Other masking materials may be used. The first mask may be patterned using standard

20   photolithography techniques and etching in a buffered HF solution. In one embodiment, the first openings **107** are 3μm-wide openings that extend in parallel at distances of between 3 and 40μm and that are oriented along the $<1\bar{1}00>$ direction on the underlying gallium nitride layer **104**. Prior to further processing, the structure may be dipped in a 50% buffered hydrochloric acid (HCl) solution to remove surface

25   oxides from the underlying gallium nitride layer **104**.

Referring now to Figure 8, the underlying gallium nitride layer **104** is grown through the first array of openings **107** to form first vertical gallium nitride layer **108a** in the first openings. Growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used

30   in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As shown in Figure 8, the first gallium nitride layer **108a** grows vertically to the top of the first mask **106**.

It will be understood that underlying gallium nitride layer **104** also may be grown laterally without using a mask **106**, by appropriately controlling growth parameters and/or by appropriately patterning the underlying gallium nitride layer **104**. A patterned layer may be formed on the underlying gallium nitride layer after

5 vertical growth or lateral growth, and need not function as a mask.

It will also be understood that lateral growth in two dimensions may be used to form an overgrown gallium nitride semiconductor layer. Specifically, mask **106** may be patterned to include an array of openings **107** that extend along two orthogonal directions such as $< 1\bar{1}00 >$ and $< 11\bar{2}0 >$. Thus, the openings can form a

10 rectangle of orthogonal striped patterns. In this case, the ratio of the edges of the rectangle is preferably proportional to the ratio of the growth rates of the $\{11\bar{2}0\}$ and $\{1\bar{1}01\}$ facets, for example, in a ratio of 1.4:1.

Referring now to Figure 9, continued growth of the first gallium nitride layer **108a** causes lateral overgrowth onto the first mask **106**, to form first lateral gallium

15 nitride layer **108b**. Growth conditions for overgrowth may be maintained as was described in connection with Figure 8.

Referring now to Figure 10, lateral overgrowth is optionally allowed to continue until the lateral growth fronts coalesce at first interfaces **108c**, to form a first continuous gallium nitride layer **108**. The total growth time may be approximately 60

20 minutes. Microelectronic devices may be formed in the first continuous gallium nitride layer **108**.

Optionally, referring now to Figure 11, the first vertical gallium nitride layer **108a** is masked with a second mask **206** that includes a second array of openings **207** therein. The second mask may be fabricated as was described in connection with the

25 first mask. The second mask may also be eliminated, as was described in connection with the first mask of Figure 8. As already noted, the second mask **206** preferably covers the entire first vertical gallium nitride layer **108a**, so as to prevent defects therein from propagating vertically or laterally. In order to provide defect-free propagation, mask **206** may extend onto first lateral gallium nitride layer **108b** as

30 well.

Referring now to Figure 12, the first lateral gallium nitride layer **108c** is grown vertically through the second array of openings **207**, to form second vertical

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gallium nitride layer **208a** in the second openings. Growth may be obtained as was described in connection with Figure 8.

Referring now to Figure 13, continued growth of the second gallium nitride layer **208a** causes lateral overgrowth onto the second mask **206**, to form second lateral gallium nitride layer **208b**. Lateral growth may be obtained as was described in connection with Figure 8.

Referring now to Figure 14, lateral overgrowth preferably continues until the lateral growth fronts coalesce at second interfaces **208c** to form a second continuous gallium nitride layer **208**. Total growth time may be approximately 60 minutes. Microelectronic devices may then be formed in regions **208a** and in regions **208b** as shown in Figure 15, because both of these regions are of relatively low defect density. Devices may bridge these regions as well, as shown. Accordingly, a continuous device quality gallium nitride layer **208** may be formed.

Additional discussion of the methods and structures of the present invention will now be provided. As described above, the openings **107** and **207** in the masks are preferably rectangular stripes that preferably extend along the $<11\bar{2}0>$ and/or $<1\bar{1}00>$ directions relative to the underlying gallium nitride layer **104**. Truncated triangular stripes having $(1\bar{1}01)$ slant facets and a narrow (0001) top facet may be obtained for mask openings **107** and **207** along the $<11\bar{2}0>$ direction. Rectangular stripes having a (0001) top facet, $(11\bar{2}0)$ vertical side faces and $(1\bar{1}01)$ slant facets may be grown along the $<1\bar{1}00>$ direction. For growth times up to 3 minutes, similar morphologies may be obtained regardless of orientation. The stripes develop into different shapes if the growth is continued.

The amount of lateral growth generally exhibits a strong dependence on stripe orientation. The lateral growth rate of the $<1\bar{1}00>$ oriented stripes is generally much faster than those along $<11\bar{2}0>$. Accordingly, it is most preferred to orient the openings **107** and **207** so that they extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104**.

The different morphological development as a function of opening orientation appears to be related to the stability of the crystallographic planes in the gallium nitride structure. Stripes oriented along $<11\bar{2}0>$ may have wide $(1\bar{1}00)$ slant facets and either a very narrow or no (0001) top facet depending on the growth conditions.

This may be because $(1\bar{1}01)$ is the most stable plane in the gallium nitride wurtzite

crystal structure, and the growth rate of this plane is lower than that of others. The

$\{1\bar{1}01\}$ planes of the $<1\bar{1}00>$ oriented stripes may be wavy, which implies the

existence of more than one Miller index. It appears that competitive growth of

5   selected $\{1\bar{1}01\}$ planes occurs during the deposition which causes these planes to

become unstable and which causes their growth rate to increase relative to that of the

$(1\bar{1}01)$ of stripes oriented along $<11\bar{2}0>$.

    The morphologies of the gallium nitride layers selectively grown on openings

oriented along $<1\bar{1}00>$ are also generally a strong function of the growth

10   temperatures. Layers grown at 1000°C may possess a truncated triangular shape. This

morphology may gradually change to a rectangular cross-section as the growth

temperature is increased. This shape change may occur as a result of the increase in

the diffusion coefficient and therefore the flux of the gallium species along the (0001)

top plane onto the $\{1\bar{1}01\}$ planes with an increase in growth temperature. This may

15   result in a decrease in the growth rate of the (0001) plane and an increase in that of

the $\{1\bar{1}01\}$. This phenomenon has also been observed in the selective growth of

gallium arsenide on silicon dioxide. Accordingly, temperatures of 1100°C appear to

be most preferred.

    The morphological development of the gallium nitride regions also appears to

20   depend on the flow rate of the TEG. An increase in the supply of TEG generally

increases the growth rate of the stripes in both the lateral and the vertical directions.

However, the lateral/vertical growth rate ratio decrease from 1.7 at the TEG flow rate

of 13μmol/min to 0.86 at 39μmol.min. This increased influence on growth rate along

<0001> relative to that of $<11\bar{2}0>$ with TEG flow rate may be related to the type of

25   reactor employed, wherein the reactant gases flow vertically and perpendicular to the

substrate. The considerable increase in the concentration of the gallium species on

the surface may sufficiently impede their diffusion to the $\{1\bar{1}01\}$ planes such that

chemisorption and gallium nitride growth occur more readily on the (0001) plane.

    Continuous 2μm thick gallium nitride layers **108** and **208** may be obtained

30   using 3μm wide stripe openings **107** and **207** spaced 7μm apart and oriented along

$<1\bar{1}00>$, at 1100°C and a TEG flow rate of 26μmol/min. The overgrown gallium

nitride layers **108b** and **208b** may include subsurface voids that form when two

growth fronts coalesce. These voids may occur most often using lateral growth

conditions wherein rectangular stripes having vertical $\{11\bar{2}0\}$ side facets developed.

The coalesced gallium nitride layers **108** and **208** may have a microscopically

flat and pit-free surface. The surfaces of the laterally grown gallium nitride layers

5   may include a terrace structure having an average step height of 0.32nm. This terrace

structure may be related to the laterally grown gallium nitride, because it is generally

not included in much larger area films grown only on aluminum nitride buffer layers.

The average RMS roughness values may be similar to the values obtained for the

underlying gallium nitride layers **104**.

10   Threading dislocations, originating from the interface between the gallium

nitride underlayer **104** and the buffer layer **102b**, appear to propagate to the top

surface of the first vertical gallium nitride layer **108a** within the first openings **107** of

the first mask **106**. The dislocation density within these regions is approximately

$10^9 cm^{-2}$. By contrast, threading dislocations do not appear to readily propagate into

15   the first overgrown regions **108b**. Rather, the first overgrown gallium nitride regions

108b contain only a few dislocations. These few dislocations may be formed parallel

to the (0001) plane via the extension of the vertical threading dislocations after a 90°

bend in the regrown region. These dislocations do not appear to propagate to the top

surface of the first overgrown GaN layer. Since both the second vertical gallium

20   nitride layer **208a** and the second lateral gallium nitride layer **208b** propagate from

the low defect first overgrown gallium nitride layer **108b**, the entire layer **208** can

have low defect density.

As described, the formation mechanism of the selectively grown gallium

nitride layer is lateral epitaxy. The two main stages of this mechanism are vertical

25   growth and lateral growth. During vertical growth, the deposited gallium nitride

grows selectively within the mask openings **107** and **207** more rapidly than it grows

on the masks **106** and **206**, apparently due to the much higher sticking coefficient "s"

of the gallium atoms on the gallium nitride surface (s=1) compared to on the mask

(s~1). Since the SiO_2 bond strength is 799.6 kJ/mole and much higher than that of Si-

30   N (439 kJ/mole), Ga-N (103 kJ/mole), and Ga-O (353.6 kJ/mole), Ga or N atoms

should not readily bond to the mask surface in numbers and for a time sufficient to

cause gallium nitride nuclei to form. They would either evaporate or diffuse along

the mask surface to the openings **107** or **207** in the masks or to the vertical gallium

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nitride surfaces **108a** or **208a** which have emerged. During lateral growth, the gallium nitride grows simultaneously both vertically and laterally over the mask from the material which emerges over the openings.

Surface diffusion of gallium and nitrogen on the masks may play a minor role

5 in gallium nitride selective growth. The major source of material appears to derived from the gas phase. This may be demonstrated by the fact that an increase in the TEG flow rate causes the growth rate of the (0001) top facets to develop faster than the $(1\bar{1}01)$ side facets and thus controls the lateral growth.

The laterally grown gallium nitride layers **108b** and **208b** bond to the

10 underlying masks **106** and **206** sufficiently strongly so that they generally do not break away on cooling. However, lateral cracking within the SiO$_2$ may take place due to thermal stresses generated on cooling. The viscosity (ρ) of the SiO$_2$ at 1050°C is about $10^{15.5}$ poise which is one order of magnitude greater than the strain point (about $10^{14.5}$ poise) where stress relief in a bulk amorphous material occurs within

15 approximately six hours. Thus, the SiO$_2$ mask may provide limited compliance on cooling. As the atomic arrangement on the amorphous SiO$_2$ surface is quite different from that on the GaN surface, chemical bonding may occur only when appropriate pairs of atoms are in close proximity. Extremely small relaxations of the silicon and oxygen and gallium and nitrogen atoms on the respective surfaces and/or within the

20 bulk of the SiO$_2$ may accommodate the gallium nitride and cause it to bond to the oxide.

Accordingly, regions of lateral epitaxial overgrowth through mask openings from an underlying gallium nitride layer may be achieved via MOVPE. The growth may depend strongly on the opening orientation, growth temperature and TEG flow

25 rate. Coalescence of overgrown gallium nitride regions to form regions with both extremely low densities of dislocations and smooth and pit-free surfaces may be achieved through 3µm wide mask openings spaced 7µm apart and extending along the $<1\bar{1}00>$ direction, at 1100°C and a TEG flow rate of 26µmol/min. The lateral overgrowth of gallium nitride via MOVPE may be used to obtain low defect density

30 continuous gallium nitride layers for microelectronic devices.

The embodiments of Figures 1-15 can use bulk (111) silicon substrate **102a**, a 3C-silicon carbide layer **102b/102c'** and a buffer layer **102d** as a platform **102** on which to grow high quality gallium nitride microelectronic layers. The silicon

carbide layer **102b/102c'** may be critical to the success of forming gallium nitride structures according to the present invention. First, silicon carbide is a preferred material template on which to grow the buffer layer **102d** and the gallium nitride semiconductor layer **104**. Moreover, the silicon carbide layer may provide a diffusion

5   barrier to prevent the interaction of silicon atoms with gallium and nitrogen species found in the growth environment. If there is no diffusion barrier or a diffusion barrier of insufficient thickness is present, then at elevated temperatures that are used for lateral epitaxial growth, the silicon atoms from the silicon substrate may have sufficient energy and mobility to diffuse to the surface of the aluminum nitride buffer

10   layer and to react with the gallium and nitrogen species in the growth environment. This may result in the formation of large voids in the underlying silicon substrate and in the "poisoning" of the gallium nitride growth, which may result in the undesirable formation of polycrystalline gallium nitride-containing structures.

Referring now to Figures 16-26, second embodiments of fabricating gallium nitride

15   microelectronic layers according to the present invention will be described. In contrast with the embodiment of Figures 1-15, the embodiments of Figures 16-26 begin with a (111) silicon SIMOX substrate **202** including a buried layer of silicon dioxide **202b** therein that define a (111) silicon surface layer **202c** on an underlying (111) silicon substrate **202a**. See Figure 16. The buried layer of silicon dioxide may

20   be fabricated by implanting oxygen into a (111) silicon substrate to define a (111) silicon surface layer on the (111) silicon substrate. This process generally is referred to as SIMOX and is described for example in a publication entitled *Silicon-on-Insulator: Why, How, and When* by Chen, AIP Conference Proceedings, Vol. 167, No. 1, September 15, 1988, pp. 310-319.

25   Then, referring to Figure 17, at least a portion of the (111) silicon surface layer **202c** is converted to 3C-silicon carbide. In Figure 17 the entire (111) silicon surface layer **202c** is converted to a layer of 3C-silicon carbide **202c'**, for example in a manner described above. As was described above, the conversion step of Figure 17 may be omitted.

30   Then, referring to Figure 18, a layer of 3C-silicon carbide **202d** is epitaxially grown on the converted (111) silicon surface layer **202c'** or directly on the (111) silicon surface layer **202c** in a manner that was described above. As shown in Figure 19, the epitaxially grown layer of 3C-silicon carbide **202d** optionally is thinned to produce a thinned epitaxial layer of 3C-silicon carbide **202d'**.

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As shown in Figure 20, a 2H-aluminum nitride layer and/or gallium nitride buffer 202e then is grown on the thinned epitaxially grown layer of 3C-silicon carbide 202d'. Then, as shown in Figure 21 an underlying layer of 2H-gallium nitride 204 is grown on the buffer layer 202e.

5   Figures 22-26 now will show the use of pendeoepitaxy to laterally grow the underlying layer of 2H-gallium nitride 204 to thereby produce a gallium nitride microelectronic layer. However, it will be understood that epitaxial lateral overgrowth techniques of Figures 7-15, and/or other techniques may be used.

Referring to Figure 22, the underlying gallium nitride layer 204 includes a

10   plurality of sidewalls 205 therein. It will be understood by those having skill in the art that the sidewalls 205 may be thought of as being defined by a plurality of spaced apart posts 206, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls 205 also may be thought of as being defined by a plurality of trenches 207, also referred to as "wells" in the underlying gallium nitride layer 204. The

15   sidewalls 205 may also be thought of as being defined by a series of alternating trenches 207 and posts 206. Moreover, a single post 206 may be provided, that may be thought of as being defined by at least one trench 207 adjacent the single post. It will be understood that the posts 206 and the trenches 207 that define the sidewalls 205 may be fabricated by selective etching, selective epitaxial growth and/or other

20   conventional techniques. Moreover, it also will be understood that the sidewalls need not be orthogonal to the substrate 202, but rather may be oblique thereto. Finally, it also will be understood that although the sidewalls 205 are shown in cross-section in Figure 22, the posts 206 and trenches 207 may define elongated regions that are straight, V-shaped or have other shapes. As shown in Figure 22, the trenches 207

25   may extend into the buffer layer 202e and into the silicon carbide layer 202c'/202d', so that subsequent gallium nitride growth occurs preferentially on the sidewalls 205 rather than on the trench floors. In other embodiments, the trenches may not extend into the silicon carbide layer 202c'/202d', and also may not extend into buffer layer 202e, depending, for example, on the trench geometry and the lateral versus vertical

30   growth rates of the gallium nitride.

Referring now to Figure 23, the sidewalls 205 of the underlying gallium nitride layer 204 are laterally grown to form a lateral gallium nitride layer 208a in the trenches 207. Lateral growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used

in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As used herein, the term "lateral" means a direction that is orthogonal to the sidewalls 205. It will also be understood that some vertical growth on the posts 206 may also take place during the lateral growth from sidewalls 205. As used herein, the term "vertical" denotes a directional parallel to the sidewalls 205.

Referring now to Figure 24, continued growth of the lateral gallium nitride layer 208a causes vertical growth onto the underlying gallium nitride layer 204, specifically onto the posts 206, to form a vertical gallium nitride layer 208b. Growth conditions for vertical growth may be maintained as was described in connection with Figure 23. As also shown in Figure 24, continued vertical growth into trenches 207 may take place at the bottom of the trenches.

Referring now to Figure 25, growth is allowed to continue until the lateral growth fronts coalesce in the trenches 207 at the interfaces 208c, to form a continuous gallium nitride semiconductor layer in the trenches. The total growth time may be approximately 60 minutes. As shown in Figure 26, microelectronic devices 210 may then be formed in the lateral gallium nitride semiconductor layer 208a. Devices also may be formed in vertical gallium nitride layer 208b.

It will be understood that in the embodiments of Figures 16-26, a mask need not be used to fabricate the gallium nitride semiconductor structures because lateral growth is directed from the sidewalls 205. However, as will be described in connection with Figures 27-41, a mask may be used. It also will be understood by those having skill in the art that in order to obtain a continuous gallium nitride layer of low crystallographic defects an epitaxial lateral overgrowth then may be performed on the structure of Figure 26 using a mask as was described in connection with Figures 7-15. Laterally offset masks also may be used. Moreover, a second, laterally offset pendeoepitaxial process may be performed on the structure of Figure 26 by defining second trenches and/or posts. By performing two separate lateral growths, the defect density may be reduced considerably.

As was described in connection with Figures 16-26, a silicon substrate containing a buried oxide layer such as a SIMOX wafer 202 is used. The use of a SIMOX wafer can prevent or limit warping of the substrate after formation of silicon carbide layers 202c'/202d'. In particular, when the structures are cooled after silicon carbide formation from growth temperatures to room temperature, the structures may

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warp due to the large mismatches in the coefficients of thermal expansion between silicon and silicon carbide. This effect may be more pronounced when using large diameter silicon wafers. To reduce this effect, using wafers with layers of oxide **202b** may prevent or reduce the warping by acting as a compliant substrate. At the

5   elevated temperatures used in silicon carbide formation, the oxide may undergo viscous flow and accommodate the mismatches in both the lattice parameters and the coefficient of thermal expansion between the silicon and the silicon carbide layers. On cooling, the oxide layer may then provide a mechanism of strain relief and limit the warping of the substrate.

10   Moreover, as described above, the silicon carbide **202c'/202d'** is a preferred material template on which to grow the aluminum nitride buffer layer **202e** and the gallium nitride semiconductor layers **204**. Pendeoepitaxial growth of gallium nitride may be obtained on silicon carbide, because under the growth conditions used for pendeoepitaxial growth, gallium and nitrogen atoms generally will not bond to the

15   silicon carbide surface in numbers and in time sufficient to cause gallium nitride nuclei to form. Finally, as described above, the silicon carbide layer may provide a diffusion barrier to prevent the interaction of silicon atoms with gallium and nitrogen species found in the growth environment.

Referring now to Figures 27-41, third embodiments according to the present

20   invention now will be described. These embodiments use a Semiconductor-On-Insulator (SOI) substrate as a platform for growth of gallium nitride microelectronic layers. As will be described in detail below, these embodiments may be particularly useful for integration of electronic devices such as conventional CMOS devices and optoelectronic devices such as gallium nitride lasers and/or LEDs.

25   Referring now to Figure 27, a plurality of microelectronic devices **301**, including but not limited conventional CMOS devices, are fabricated in a (100) silicon substrate **302a** using conventional techniques. It will be understood that the devices **301** may be formed later as well, as will be described in detail below. It also will be understood that microelectronic devices **301** may include optical and/or

30   microelectromechanical (MEMS) devices as well.

Referring to Figure 28, the (100) silicon substrate **302a** then is bonded to a (111) silicon substrate **302c** using a bonding layer **302b** and conventional bonding techniques. The bonding layer may be a microelectronic epoxy, a layer of silicon dioxide and/or other conventional materials. Then referring to Figure 29, the (111)

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silicon substrate **302c** is thinned to produce a (111) silicon layer **302c'** on the (100) silicon substrate **302a**. The operations of Figures 27-29 may form a conventional silicon on insulator (SOI) substrate **302** except that microelectronic devices **301** are contained therein.

5   Referring now to Figure 30, at least part of the (111) silicon layer **302c'** is converted to 3C-silicon carbide layer **302c''**. As shown in Figure 30, all of the layer **302c'** is converted to silicon carbide layer **302c''**. Moreover, as was described above, the conversion step may be eliminated. Then, as shown in Figure 31, a layer of 3C-silicon carbide **302d** may be epitaxially grown on the converted (111) silicon layer

10   **302c''**. Optionally, as shown in Figure 32, the epitaxially grown layer of 3C-silicon carbide **302d** is thinned to produce thinned layer **302d'**. An aluminum nitride layer **302e** then is grown on a thinned epitaxially grown layer of 3C-silicon carbide **302d'**. This provides a platform **302'** for subsequent growth of gallium nitride. As shown in Figure 34, a layer of 2H-gallium nitride **304** is grown on the aluminum nitride layer

15   **302e**.

In Figures 35-39, masked pendeoepitaxy is performed to laterally grow the layer of 2H-gallium nitride **304** to produce a gallium nitride microelectronic layer. However, it will be understood that maskless pendeoepitaxy, epitaxial lateral growth, other techniques and/or combinations thereof also may be used.

20   Referring now to Figure 35, a mask such as silicon nitride mask **309** is provided on the underlying gallium nitride layer **304**. The mask **309** may have a thickness of about 1000 Ångstroms and may be formed on the underlying gallium nitride layer **304** using low pressure chemical vapor deposition (CVD) at 410°C.

Still referring to Figure 35, the underlying gallium nitride layer **304** includes a

25   plurality of sidewalls **105** therein. As already described, it will be understood by those having skill in the art that the sidewalls **305** may be thought of as being defined by a plurality of spaced apart posts **306**, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls **305** may also be thought of as being defined by a plurality of trenches **307**, also referred to as "wells" in the underlying gallium

30   nitride layer **304**. The sidewalls **305** may also be thought of as being defined by a series of alternating trenches **307** and posts **306**. It will be understood that the posts **306** and the trenches **307** that define the sidewalls **305** may be fabricated by selective etching, selective epitaxial growth and/or other conventional techniques. Moreover,

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it also will be understood that the sidewalls need not be orthogonal to the substrate 302, but rather may be oblique thereto. Finally, it will also be understood that although the sidewalls 305 are shown in cross-section in Figure 35, the posts 306 and trenches 307 may define elongated regions that are straight, V-shaped or have other shapes. As shown in Figure 35, the trenches 307 preferably extend into the buffer layer 302e and into the silicon carbide layer 302d'/302c'', so that subsequent gallium nitride growth occurs preferentially on the sidewalls 305 rather than on the trench floors. In other embodiments, the trenches may not extend into the silicon carbide layer 302d'/302c'', and also may not extend into the buffer layer 302e.

Referring now to Figure 36, the sidewalls 305 of the underlying gallium nitride layer 304 are laterally grown to form a lateral gallium nitride layer 308a in the trenches 307. Lateral growth of gallium nitride may be obtained at about 1000-1100°C and about 45 Torr. The precursors TEG at about 13-39μmol/min and NH$_3$ at about 1500 sccm may be used in combination with about 3000 sccm H$_2$ diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, also may be used. As used herein, the term "lateral" means a direction that is parallel to the faces of the substrate 302'. It will also be understood that some vertical growth of the lateral gallium nitride 308a may also take place during the lateral growth from the sidewalls 305. As used herein, the term "vertical" denotes a directional parallel to the sidewalls 305.

Referring now to Figure 37, continued growth of the lateral gallium nitride layer 308a causes vertical growth of the lateral gallium nitride layer 308a. Conditions for vertical growth may be maintained as was described above. As also shown in Figure 37, continued vertical growth into trenches 307 may take place at the bottom of the trenches.

Referring now to Figure 38, continued growth of the lateral gallium nitride layer 308a causes lateral overgrowth onto the mask 309, to form lateral overgrowth gallium nitride layer 308b. Growth conditions for overgrowth may be maintained as was described above.

Referring now to Figure 39, growth is allowed to continue until the lateral growth fronts coalesce in the trenches 307 at the interfaces 308c, to form a continuous gallium nitride semiconductor layer in the trenches.

Still referring to Figure 39, growth is allowed to continue until the lateral overgrowth fronts coalesce over the mask 309 at the interfaces 308d, to form a

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continuous gallium nitride semiconductor layer. The total growth time may be approximately 60 minutes. As shown in Figure 40, microelectronic devices **310** may then be formed in the lateral gallium nitride semiconductor layer **308a**. Devices may also be formed in lateral overgrown gallium nitride layer **308b**.

5   Then referring to Figure 41, at least a portion of the 3C-silicon carbide layer **102c"/102d'**, the aluminum nitride layer **302e**, the gallium nitride layer **304** and the microelectronic layer **308** are removed to expose the microelectronic devices **301** in the (100) silicon substrate. The microelectronic devices **301** in the (100) silicon substrate then may be electrically connected to the microelectronic devices **310** in the

10   pendeoepitaxial gallium nitride layer to provide an integrated optical and electronic substrate. The connection may use conventional metalization soldering and/or other techniques. Accordingly, high density integrated optoelectronic devices may be formed using conventional (100) silicon SOI substrates.

          As was described in connection with the embodiment of Figures 16-26, the

15   silicon carbide layer **302d'/302c"** may be critical to the success of forming gallium nitride structures because the silicon carbide is a preferred material template on which to grow the aluminum nitride layer **302e** and the gallium nitride semiconductor layer **304**. Moreover, under the growth conditions used for pendeoepitaxial growth, gallium and nitrogen atoms generally will not bond to the silicon carbide surface in

20   numbers and times sufficient to cause gallium nitride nuclei to form. Alternatively, it will be understood that the bottom of the trenches **307** may be masked, for example with silicon nitride. The silicon carbide layer also may provide a diffusion barrier to prevent the interaction of silicon atoms with gallium and nitrogen species found in the growth environment.

25   Moreover, as was described above, the SOI wafers can prevent or limit warping of the substrate after silicon carbide formation. In particular, the bonding layer **302b** may prevent or limit the warping by acting as a compliant substrate. On cooling, the bonding layer **302b** may also provide a mechanism of strain relief and may limit the warping of the substrate.

30   Referring now to Figures 42-45, other embodiments of gallium nitride semiconductor structures and fabrication methods according to the present invention will now be described. The structures use different spacings or dimensions for the posts and trenches. In Figures 42 and 43, a small post-width/trench width ratio is used. Thus, discreet gallium nitride structures shown in Figure 42 may be obtained.

In another embodiment, a large post-width/trench-width ratio is used so that gallium nitride structures shown in Figure 44 may be obtained.

Referring now to Figure 42, using a small post-width/trench-width ratio, gallium nitride semiconductor structures of Figure 42 are fabricated as was already described. Still referring to Figure 42, growth is allowed to continue until the lateral overgrowth fronts coalesce over the mask **309** at the interface **308b** to form a continuous gallium nitride semiconductor layer over the mask **309**. The total growth time may be approximately 60 minutes. As shown in Figure 42, microelectronic devices **310** may be formed in the lateral overgrowth gallium nitride layer **308d**. Then, as shown in Figure 43, at least some of the discreet gallium nitride structures are removed to expose the microelectronic devices **301** in the (100) silicon substrate **302a**.

Referring now to Figure 44, using a large post-width/trench-width ratio, gallium nitride semiconductors structures of Figure 44 are fabricated as was already described. Still referring to Figure 44, growth is allowed to continue until the lateral overgrowth fronts coalesce in the trench **307** at the interfaces **308c** to form a continuous gallium nitride semiconductor layer **308a** over the trench **307**. The total growth time may be approximately 60 minutes. As shown in Figure 44, microelectronic devices **310** may be formed in the pendeoepitaxial gallium nitride layer **308a**. Then, as shown in Figure 45, at least a portion of the gallium nitride structure may be removed to thereby expose the underlying microelectronic devices **301**, and was described above.

In the above-described embodiments, devices **301** are formed in the (100) silicon substrate **302a** prior to forming the gallium nitride devices **310**. However, it will be understood that gallium nitride fabrication processes may occur at temperatures that are sufficiently high to destroy or degrade performance of the silicon devices **301** due to diffusion or other thermal effects. Accordingly, it may be desirable to form the microelectronic devices **301** in the (100) silicon substrate **302a** after forming the gallium nitride layers and structures.

Figures 46-49 illustrate methods of forming microelectronic devices in the (100) silicon substrate after forming the gallium nitride layers and structures. In particular, as shown in Figure 46, the structure of Figure 45 may be fabricated except that microelectronic devices **301** are not formed until after the gallium nitride structures are formed. Thus, as shown in Figure 46, upon removal of at least some of

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the gallium nitride structures, the face of the (100) silicon substrate **302a** is exposed, and conventional microelectronic devices **301** may be formed in the exposed surface.

It may be difficult to fabricate the microelectronic devices **301** within the trenches between the gallium nitride devices. The embodiments of Figures 47-49

5 illustrate alternative fabrication techniques that need not fabricate the silicon microelectronic devices **301** at the bottom of the trenches.

In particular, referring to Figure 47, the device of Figure 45 is fabricated except that microelectronic devices **301** are not fabricated in the (100) silicon substrate **302a**. A capping layer **320**, for example silicon dioxide and/or silicon

10 nitride, then is formed on the gallium nitride devices. Then, referring to Figure 48, the (100) silicon substrate **302a** is selectively epitaxially grown to form a (100) silicon layer **302a'**. Devices **301'** then are formed in the epitaxially grown silicon layer **302a'**. Thus, the devices **301'** may be formed at the surface of the structure rather than at the floor of a trench.

15 Finally, as shown in Figure 49, the capping layer **320** optionally may be removed to provide a free-standing silicon layer **302a'** that is separated from the gallium nitride-based structures. The devices may be connected using metallization at the top surface. Alternatively, metallization within or on the (100) silicon substrate **302a** may be provided.

20 In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation.